IN THE CLAIMS:

Please cancel Claims 12 and 15 without prejudice or disclaimer.

Please amend Claims 14 and 19 as follows:

14. (Twice amended) A computer graphics processor system having the capability of mapping texture onto a three dimensional object in a scene being displayed, the system comprising:

a texture address calculator for generating texel addresses for a list of primitives being processed;

a texture main memory containing an array of texels, each texel having an address and one of N identifiers;

a texture cache memory having addresses partitioned into N banks, each bank containing texels transferred from said main memory that have the corresponding identifier;

a texture cache controller for determining and requesting the necessary transfer of texels from said texture main memory addresses to said texture cache memory addresses; and

a texture cache arbiter for scheduling and controlling the actual transfer of texels from said texture main memory into the texture cache memory and controlling the outputting of texels for each pixel to a interpolating filter from the cache memory, said cache arbiter coupled between said controller and said texture cache memory for determining which texels in the cache memory can be overwritten when new texels are determined to be transferred to said cache memory by said cache controller, said texture

cache arbiter transfers said texels from said texture main memory into the cache memory according to a look-ahead algorithm to hide read and write access clock cycles between sequential pixels.

19. (Amended) A computer graphics processor system having the capability of mapping texture onto a three dimensional object in a scene being displayed, the system comprising:

a texture address calculator for generating texel addresses for a list of primitives being processed;

a texture main memory containing an array of texels, each texel having an address and one of N identifiers;

a texture cache memory having addresses partitioned into N banks, each bank containing texels transferred from said main memory that have the corresponding identifier;

a texture cache controller for determining and requesting the necessary transfer of texels from said texture main memory addresses to said texture cache memory addresses, said cache controller including a plurality of least recently used controllers coupled in succession to thereby transfer texels according to a least recently used replacement algorithm, said texture cache controller pre-fetching necessary neighboring texels from said texture main memory for bilinear texture filtering; and

a texture cache arbiter for scheduling and controlling the actual transfer of texels from said texture main memory into the texture cache memory and controlling the outputting of texels for each pixel to a interpolating filter from the cache memory.